

**CD21/2140 and CD21/2141
128K-2M Parity Checking
Dynamic RAM Boards**

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1. General Information

Distinctive Characteristics

- * Dynamic RAM--low power consumption
- * 170ns typical read data available time; 135ns for fast version
- * Parity checking is standard
- * Increased noise immunity from multi-layer PC board
- * External battery backup capability
- * Decodes the full 24-bit address bus
- * Error detection I/O port with 8- or 16-bit addressing

The CD21/2140 and CD21/2141 128K-2M Parity Checking Dynamic RAM boards (jointly referred to as CD21/214X) allow the user to add 128K, 256K, 384K, or 512K of RAM (512K, 1 megabyte, or 2 megabytes for 256K RAMs) to any Multibus¹ system. Completely Multibus compatible, this board runs at a maximum data access time of 205ns and a maximum XACK return time of 230ns (155ns and 175ns, respectively, for faster version). The board can operate in 8- or 16-bit mode, depending on the Multibus BHEN signal.

The board decodes the full 24-bit address bus, allowing a system-wide memory address capacity of 16 megabytes. The board is divided into two sections, each of which can be addressed on a 256K memory boundary (1 megabyte boundary with 256K RAMs). Additionally, each row of memory devices may be disabled by removing one of four row enable jumpers.

The on-board refresh arbitration circuitry is designed to minimize wait-states caused by refresh cycles which are normally initiated every 15 microseconds. If the processor accesses another board in this system at any time between refresh cycles, a new refresh cycle is initiated to overlap that memory cycle (given hidden refresh). Also, refresh cycles are hidden between access cycles to the board.

The board provides parity checking which can be used to alert the user or host computer of a memory error. When a parity error occurs, the group of RAMs which caused the error can be determined by three LEDs mounted on the top of the board. An error reset button is also provided to clear the error condition. The user can also select that the occurrence of a parity error will generate an interrupt on any of the Multibus vectored interrupt lines.

¹Multibus is a trademark of Intel Corporation.

When the processor is interrupted because of a parity error, it can read an I/O port on the board to determine which group of RAMs failed. By writing to the same port address, the error condition can be cleared and the interrupt removed. This I/O port address can be decoded using either an 8- or 16-bit address.

The board drives both the XACK and AACK signals of the Multibus to allow for the greatest flexibility. It returns XACK when the data transfer is complete, while AACK may be jumpered by the user to return a fixed amount of time before XACK. When AACK is jumpered properly, it allows the fastest possible system operation.

2. Functional Description

This chapter provides a functional description of the CD21/214X. In this manual, both active-high and active-low signals appear in the text. Whenever a signal is active-low, its mnemonic is followed by a slash (/).

Memory Address Comparators

This board allows two independent DIP switch-addressable 256K memory sections.

The three configuration jumpers labeled 64 should be installed for boards using 64K devices; the jumper labeled 256 should be installed for boards using 256K devices. The two sets of jumpers should never be installed at the same time.

Each of the two comparators performs a bit-for-bit comparison between its 6-position DIP switch and address lines A18/-A23/. Note that boards with 256K RAMs use only four of the comparator's inputs; therefore, the switches for the unused two inputs should be left open.

Cycle/Refresh Arbiter

The Cycle/Refresh Arbiter initiates both memory and refresh cycles; in the case of a conflict, it determines which cycle will be performed first.

When either MRDC/ or MWRC/ is asserted, the COMD line switches high, indicating that a system memory cycle is in progress. This low to high transition latches the state of the MSEL line into pin 8 of IC99 to determine if the memory cycle is addressed to this board (if pin 8 is low).

When a refresh cycle is required, the state of the COMD line is latched into pin 5 of IC99 by the low to high transition of the START REFRESH signal which selects either pin 6 or pin 8 of IC111 to start the refresh cycle. If COMD was low (indicating no memory cycle is in progress), pin 6 of IC99 will be high, and the refresh cycle will be initiated by the low to high transition of the delayed START REFRESH signal.

If COMD was high (indicating a system memory cycle is in progress), pin 5 of IC99 will be high. If pin 8 of IC99 is low (indicating a memory cycle to this board), the refresh cycle will be held off until the memory cycle is complete and pin 8 of IC99 has been set.

The two delay lines of IC100 prevent glitches on the START/ line (pin 8 of IC105) when simultaneous memory and refresh requests occur.

When START REFRESH and COMD both switch high at approximately the same time, the data setup and/or hold times at pin 2 of IC99 will be violated, and IC99 may enter an unstable condition. The START REFRESH signal is delayed by 16ns

and is used to hold off the refresh starting gates, providing a minimum of 15ns settling time for the flip-flop.

When simultaneous memory and refresh requests occur, it is uncertain which request will be processed first. Therefore, the start of the memory cycle must be delayed until the arbiter has made its choice. The COMD line is delayed by 21ns to produce the CYCLE signal, which is used to start memory cycles. The minimum delay from COMD to CYCLE is 23ns, while the maximum delay from the rising edge of START REFRESH to the falling edge of pin 6 of IC111 is 22.3ns. Since memory cycles will be inhibited when either pin 6 or pin 8 of IC111 is low, these delays will prevent false triggering of the START/ line.

Memory Cycle Timing and Control Circuitry

Memory cycles are initiated by the falling edge of START/, and the memory cycle timing is controlled by the delay line at IC97 and its associated circuitry.

At the start of a memory cycle, the 24 address lines are input to the board. The buffered row address lines (BA1-BA8, and BA17 for 256K devices) are applied to the DRAM address inputs, while address lines A17/-A23/ are decoded by the memory address decoder circuit to produce the MSEL and row enable outputs. The row enable outputs pass through a 74F158 multiplexer (IC94) to the four pairs of NAND gates (IC89, IC90, IC92, and IC93) used to drive the RAS/ inputs of the DRAMs. Each output of IC94 controls one row of RAM chips, and each of the four-input NAND gates drives nine devices (half a row). Before the start of a cycle, the COMD, DLY COMD, and CYCLE lines will all be low, preventing the start of a memory cycle and providing the following preset conditions:

1. BDSEL is low, indicating board is deselected.
2. HOLD is low, allowing memory cycles to be initiated.

Next, the MRDC/ or MWRC/ signal occurs at least 50ns after the address lines are valid, causing COMD to switch high. DLY COMD switches from low to high 21ns later, which causes CYCLE to switch high. Assuming that a refresh cycle is not in progress, the two RAS drivers selected by IC94 will be enabled, and START/ will switch low, initiating the memory cycle. START/ is inverted and used to set pin 8 of IC108 (BDSEL/).

IC97 is a 4-tap delay line, which generates the required memory timing signals. Each output provides a fixed amount of delay from the input. The high to low transition of the third tap (CK ERR/) sets IC109 (END CYCLE/), which causes the input of the delay line (START/) to switch high again, producing a negative pulse with a width of 130.5-155.5ns (88-112ns for faster version) at the input to the delay line. Each tap of the delay line is simply a shifted version of this pulse. The active delays for this delay line are as follows:

<u>Signal Name</u>	<u>Output Tap Number</u>	<u>Standard Delay (ns)</u>	<u>Faster Delay (ns)</u>
R/C/	T1	27.5 \pm 3.0	15.5 \pm 3
CASEN/	T2	53.0 \pm 4.5	33.5 \pm 4
CK ERR/	T3	133.0 \pm 6.5	90.0 \pm 6
LATCH DATA/	T4	166.0 \pm 7.0	114.0 \pm 6

The falling edge of R/C causes the column addresses (BA8-BA16, and BA18 for 256K devices) to be switched to the RAMs.

When CASEN/ switches low, CAS (pin 2 of IC98) switches high, enabling the column address strobe to the RAMs.

The high to low transition of LATCH DATA/ sets HOLD, causing pin 5 of the row decoder (IC106) to switch low, removing the RAS/ input to the RAMs. HOLD is also used to generate the XACK signal.

The rising edge of R/C causes CAS to switch low, removing the CAS/ inputs to the DRAMs.

The rising edge of CK ERR/ is used to latch the parity error status into IC121.

AACK Circuitry

The preset input of flip-flop IC108 may be connected to one of the four delay line outputs by adding a jumper to one pair of pins labeled 85, 145, 165, or 195. The values listed are the maximum amount of time that the AACK signal will be generated on the bus prior to a normally generated XACK signal. This advanced acknowledge, if used, can be sent to either the XACK pin of the Multibus or the AACK pin of the bus (with the XACK pin still being used for the normal acknowledge signal).

If one of the AACK time adjustment jumpers has been installed, pin 5 of IC108 will switch high when the appropriate delay line output switches low, causing pin 7 of IC140 to switch low. If the AACK ENBL jumper is installed, the AACK signal will be generated on the bus. If the PREACK jumper is installed, the signal will be used to generate XACK on the bus.

Refresh Timing and Control Circuitry

Sheet 2 of the schematics contains the refresh timer (IC148), which generates the REF REQ and FORCED RFSH/ signals used to initiate refresh cycles.

IC148 is a dual 4-bit binary counter, configured as an 8-bit binary counter. The counter is incremented by each high to low transition of the 4.9152MHz crystal oscillator (IC149) output. After 64 transitions of the oscillator output, the Q6 output of IC148 will switch from low to high, and REF REQ (pin 5 of IC137) will

switch high, allowing hidden refresh cycles to be initiated. With REF REQ high, the refresh counter (IC148) will again count from 0 to 56, at which time, pin 6 of IC138 will switch high, clocking REF REQ into pin 8 of IC137, generating a forced refresh condition. If a refresh cycle is initiated at any time after the REF REQ signal is generated, IC137 will be reset, thereby preventing the forced refresh cycle.

Sheet 1 of the schematics contains the refresh timing circuitry and the circuit used to initiate hidden refresh cycles. When COMD switches high, the state of the REF REQ line is latched into pin 5 of IC110. REF REQ is totally asynchronous to COMD, so pin 5 of IC110 may be unstable for a short period of time after the clock transition. When DLY COMD switches high, the state of pin 5 of IC110 is clocked into pin 8 of IC110, generating the HIDDEN RFSH/ signal. If the memory cycle in progress has been issued to another board in the system, the refresh cycle on the CD21/214X will overlap the memory cycle to the other board. If, however, the memory cycle has been issued to this board, pin 8 of IC99 will serve to hold off the refresh cycle until pin 8 of IC99 has been set.

When either HIDDEN RFSH/ or FORCED RFSH/ switches low, START REFRESH (pin 3 of IC103) switches high and the cycle/refresh arbiter takes over as previously described. After some delay, the arbiter will cause either pin 6 or pin 8 of IC111 to switch low, preventing the start of a memory cycle and setting IC115, which produces the REFRESH/ signal. The falling edge of REFRESH/ starts the timing sequence for the refresh cycles, which is controlled by the delay line at IC104.

This 5-tap delay line generates the required timing signals for the refresh cycles. Each output provides a fixed amount of delay from the input. The high to low transition of the fifth tap resets IC115, causing the input to the delay line (REFRESH/) to switch high again, producing a negative pulse of 393-441ns (184-210ns for faster version) at the input to the delay line. Each tap of the delay line is simply a shifted version of this pulse. The active delays for IC104 are as follows:

<u>Signal Name</u>	<u>Output Tap Number</u>	<u>Standard Delay (ns)</u>	<u>Faster Delay (ns)</u>
RFSH/NORM/	T1	45.0 \pm 2.5	28.0 \pm 3.7
HOLD START/	T2	65.0 \pm 3.0	43.0 \pm 4.0
----	T3	105.0 \pm 5.0	50.0 \pm 4.0
----	T4	300.0 \pm 15.0	162.0 \pm 9.0
----	T5	410.0 \pm 20.0	190.0 \pm 9.0

When IC115 is set, the rising edge of REFRESH causes CYCLE to switch high, and the falling edge of REFRESH/ starts the refresh timing sequence. The REFRESH line also controls the select input of three 74S157 quad 2-input multiplexers (shown on sheet 3 of the schematics), which select between the row address lines (for memory cycles) and the refresh counter lines (for refresh cycles). When

RFSH/NORM/ switches low, START/ will be further disabled and the select input line to IC94 will switch low, selecting the "A" inputs which are controlled by RSTROBE/. The RSTROBE/ line will initially be high, causing the four outputs of IC94 to be low, disabling the RAS drivers.

When HOLD START/ switches low, the HIDDEN REFRESH and the START REFRESH flip-flops (IC110 and IC99) are reset.

After taps 1 and 2 of the delay line have switched low, pins 6 and 8 of IC111 and CYCLE will be high, allowing the RAS drivers to be enabled entirely under the control of IC94. Taps 1 and 2 prevent memory cycles from being initiated by forcing START/ high.

When tap 3 of the delay line switches low, RSTROBE/ (pin 6 of IC103) will go low, causing all four outputs of IC94 to switch high, enabling all eight RAS drivers. When the RAS/ outputs switch low, the refresh address will be strobed into all four rows of RAM chips.

When tap 4 switches low, RSTROBE/ will switch high, removing the RAS/ inputs from the RAM chips.

When tap 5 switches low, IC115 is reset and REFRESH switches low. This causes CYCLE to switch low and the address multiplexer to again select the row address lines. REFRESH/ switching high removes the active-low input to the delay line. When RFSH/NORM/ switches high, the outputs of IC94 will follow the "B" inputs (row select inputs).

The refresh cycle is completed with the low to high transition of the HOLD START/ line. When HOLD START/ switches high, START/ will switch low if an impending memory cycle is to be performed.

In conclusion, the refresh address setup time and RAS precharge time for the refresh cycle are guaranteed by the delay from the falling edge of REFRESH/ to the falling edge of RSTROBE/. The RAS/ signal is initiated by tap 3 of the delay line and removed by tap 4, while the row address setup time and RAS precharge time for the impending memory cycle are guaranteed by the delay from the rising edge of REFRESH/ to the rising edge of HOLD START/.

Multibus Interface Logic

Sheet 2 of the schematics contains the Multibus interface logic. Three 8-bit data paths are required to interface the internal data bus with the Multibus data lines. For word operations, two buffers are used; for byte operations, a third 8-bit data path is required between internal data bus lines 8-15 and Multibus bus lines 0-7.

Three 74LS244 tri-state non-inverting octal buffers are used to enable data transfers into the board (write cycles), while three 74F373 tri-state octal latches enable

data transfers out of the board (read cycles). Each of the six devices for data I/O is enabled independently with enable lines EN1/-EN6/.

Parity Checking

In order to minimize problems of improper data causing damage to an executing program, parity checking is a standard feature of the board. The parity circuitry generates an odd parity bit for any write cycle to the board and checks that bit when any locations are read. Parity is generated on a byte basis (a requirement since the Multibus allows 8- or 16-bit transfers), with IC9, IC18, etc. being used to hold the parity data. Odd parity is defined as an odd number of bits being high in the data byte and its associated parity bit.

The parity generating/checking circuitry is shown on sheet 2 of the schematics, with the main elements being the 74F280 parity generators. These circuits have eight inputs (which are tied to the data portions of the internal data bus) and one output. The output is high when the parity of the input lines is even (an even number of bits high). These outputs are run to the data input lines of the parity RAMs, and they cause odd parity to be stored (since it is storing a bit disruptive of the even parity).

On read cycles, the parity bit read from the RAMs is compared with the bit generated by the 74F280. If the two bits do not match, one of the exclusive OR gates (IC101) will show the error. Note that the error indication does not become valid until the access time of the RAM chips has been met. When the board is selected, and it is in a read cycle, and the access time has been met (with XACK high), pin 6 of IC121 will go low. This latches pertinent data into the 74F175 latch (IC112) and the flip-flop (IC121).

The data stored in the parity latches allows the failing RAM to be traced to one of the eight groups of RAMs on the board. The output of the latch is a binary coded pointer to the group of RAMs which failed.

The signals which are latched are ROW SELECT (to determine which row in a 256K section triggered the error), SEL HI/ (to indicate which 256K section was being accessed), and the signal from pin 6 of IC101 (which is high when the error occurred in an odd byte of memory). When the three bits are used to form a code; the group of RAMs which failed can be located by reading the code from the LEDs or data bits 0-2 of the board's input port.

<u>LED Code</u>	<u>Input Port Code</u>	<u>Failed Dynamic RAM Section</u>
0	7	IC1-IC9
1	6	IC10-IC18
2	5	IC19-IC27
3	4	IC28-IC36
4	3	IC37-IC45
5	2	IC46-IC54

6	1	IC55-IC63
7	0	IC64-IC72

When the parity error flip-flop (IC121) is set, the ERROR output is used to generate the interrupt, and the ERROR/ output prevents the parity status latches from being updated. An error has occurred only when the ERROR LED is on (or when data bit 3 of the input port is set). During all other times, the latched LED error code and data bits 0-2 of the input port are meaningless.

An error reset button is provided on the top of the board to clear the outputs of the latches. A write to the board's output port will cause the same result. Also, the error latches are cleared during system reset.

It should be noted that for the parity circuit to work properly, each location of memory must first be written before it is read to prevent random errors from occurring. This can be done during initialization by clearing all memory locations.

Battery Backup Operation

The CD21/214X is designed to accommodate an external battery source for battery backup operation. An external power source of +5V $\pm 5\%$ may be applied through either pins 1-4 of P2 or pins 1-4 of an auxiliary connector at the top of the board (J3).

When entering the power down mode, MPRO/ must switch low at least 10 microseconds prior to the power being removed. When MPRO/ switches low and a jumper is installed on the option pins labeled PWR DWN, pin 4 of IC127 will switch high. If the board is not in the middle of an access cycle, pin 5 of IC127 will also switch high, causing PWR DWN/ (pin 6 of IC127) to switch low, preventing further memory access cycles. If the board is in the middle of an access cycle when the MPRO/ signal switches low, the PWR DWN/ signal will be held off until the end of the access cycle (START/ switches high).

There are two 5V power distribution busses on the CD21/214X, labeled Vcc and Vbb. The circuits powered by Vbb must be maintained during the power down condition to preserve the memory in the RAM array, while the circuits powered by Vcc only require power during normal operation. A switch is provided to short the Vbb power plane to the Vcc power plane for normal operation (without the use of the external battery supply). When the battery backup option is used, the switch should be placed to the off position, isolating the Vcc and Vbb power planes.

3. Installation

Unpacking and Inspection

Immediately upon receipt, inspect the shipping carton for evidence of mishandling during transit. If the carton is damaged or water-stained, request the carrier's agent to be present when the carton is opened. If the carrier's agent is not present and the contents are damaged, retain the carton and packing material for the agent's inspection. Shipping damages should be immediately reported to the carrier.

Central Data suggests that shipping cartons and packing material be saved in case the board must be re-shipped in the future.

Service and Repair Assistance

Service and repair assistance can be obtained from Central Data by requesting a Returned Materials Authorization (RMA) number by calling: (217) 359-8010.

Always contact Central Data before returning a product for service or repair. Before calling, have the necessary information ready:

1. part and serial number of the board,
2. purchase order number, for repair and shipping charges,
3. your shipping and billing address, and
4. your contact name and telephone number.

If the product is being returned due to damage during shipment or the product is out of warranty, a purchase order is required before repairs can be initiated.

Before shipping, remove all user modifications. Protect the equipment from damage in transit:

1. Boards should be placed in anti-static bags,
2. Allow room in the box for protective padding,
3. Forward the product and all correspondence to:

Central Data Corporation
RMA # _____
1602 Newton Drive
Champaign, IL 61821-1098

Damage sustained due to improper packaging for the return could result in extra repair charges.

Cooling Requirement

The CD21/214X Dynamic RAM board dissipates a maximum of 13W of heat. To dissipate this heat and prevent possible heat damage to the board, you must provide adequate air circulation to prevent the ambient air around the board from rising above 55°C (131°F). Typically, a minimum air flow of 200 linear feet per minute provides enough air circulation to maintain the air temperature around the board within this limit.

Configuration Jumpers

Four configuration jumpers are used to configure the board to accept 64K or 256K dynamic RAM chips. The three configuration jumpers labeled 64 should be installed for boards using 64K RAMs; the jumper labeled 256 should be installed for boards using 256K devices.

Row Enable Jumpers

Each row of RAMs has a row enable jumper which should be installed if that row of devices is to be enabled. The four row enable jumpers are labeled EN1-EN4.

Memory Address

Each half (top and bottom) of the board is addressed independently by DIP switches to start on any 256K boundary (1 megabyte boundary for 256K RAMs) in a 16 megabyte system address space.

The memory is addressed by setting switches for the top or bottom rows of memory. The top two rows are addressed with DIP switch IC119, while the bottom two rows of RAMs are addressed with DIP switch IC150. Also marked on the board are indications of the address line corresponding to each switch position, as well as the polarity of the switches. Address 23 is selected by the leftmost switch, while address 18 is selected by the rightmost. When a switch is closed, the corresponding address line is compared for 1. When the switch is open, the line is compared for 0. If only one row of either half is being used, then you must make sure that the memory chips are in the proper sockets for selection, and the row enable jumpers are enabled or disabled accordingly. If the lower 128K (or 512K) half is desired, then the chips should reside in the top row for the section. If the upper 128K (or 512K) half is desired, the chips should be moved to the bottom row of the section.

I/O Address

The board provides a parity error detection I/O port. The base address for the I/O port may be set on any one-port boundary within a 64K address space. An 8-position DIP switch (IC95) is provided to select address lines 0-7, while another 8-position DIP switch (IC128) is provided to select address lines 8-15. As in the memory addressing, the address line number and polarity for each switch is silkscreened on the board. A jumper block labeled EXT I/O or 8-BIT I/O is provided to select

between 16-bit and 8-bit I/O addressing, respectively. One of these two positions must be jumpered.

Interrupt Selection

The parity error interrupt can be gated to any of the Multibus vectored interrupt lines. The selection of which interrupt line to use is made with a jumper placed over the corresponding set of pins. These pins are labeled 0-7 and are located near the P1 connector in the center of the board.

If the user does not desire errors to generate interrupts, no jumper should be installed on the interrupt pins.

Advanced Acknowledge Jumpers

The advanced acknowledge jumpers allow the user to maximize system throughput by fine-tuning the acknowledge time of the board to overlap the overhead of the fastest master in the system.

This feature violates the Multibus specification by returning an acknowledgement before data is guaranteed to be available. A close analysis of the timing of all masters in the system is required if it is to be used.

For normal (legal) operation, the PREACK/XACK jumper array should be strapped to the XACK position, and the AACK ENBL jumper should be removed. In this configuration, the advanced acknowledge feature will be disabled, and the XACK signal will not appear on the bus until data is guaranteed to be valid on the bus for read cycles or is accepted by the board for write cycles.

For systems that support the AACK signal, the AACK feature may be enabled by installing a jumper on the AACK ENBL pins and one of the four sets of advanced acknowledge time select pins (85, 145, 165, or 195). This will cause the AACK signal to appear on the bus 85, 145, 165, or 195ns (maximum) ahead of the XACK signal.

For systems that do not support the AACK signal, the advanced acknowledge can be placed on the XACK signal of the Multibus. Its operation is identical to the AACK feature with the exception that the circuit generates the XACK signal early rather than generating both an early AACK and a normal XACK. For this option, install the PREACK/XACK jumper on PREACK and leave the AACK ENBL jumper off. Again, one of the four sets of advanced acknowledge time select pins must be jumpered.

The four possible AACK/PREACK settings are marked: 85, 145, 165, and 195. The values listed indicate the maximum value that the AACK/PREACK signal will appear before data is actually valid on the bus. Typically, the amount of pre-acknowledgement will be less than the value selected. By using the maximum values listed, however, proper operation can be guaranteed.

There are two methods for determining the proper AACK/PREACK time:

1. The recommended procedure is to determine the worst case minimum amount of overhead of the fastest master in the system, and then select AACK/PREACK time that is equal to or less than that amount of overhead. Overhead is defined as the minimum time between the sampling of the XACK or AACK and when the data is actually read by the processor.

Example: A system with two masters

1. CPU Board Minimum Overhead: 150ns
2. Hard Disk Controller Minimum Overhead: 100ns

Proper AACK/PREACK Setting: 85ns

2. The second (and least desirable) method is to initially select an AACK/PREACK time of 195ns and test the system. If improper results are returned, decrease the AACK/PREACK time to the next tap and repeat the test, until proper operation occurs. This method does not give a proper analysis which would guarantee operation under all conditions.

Test Options

Under normal conditions, the two sets of TST ERR jumpers must be installed. For testing purposes, errors may be forced in either half of the board by removing the appropriate TST ERR jumper.

Battery Backup Operation

If an external Vbb power source is driving the board using pins 1-4 of P2 or pins 1-4 of J3, then the switch above IC149 should be turned off. If all power to the board is being supplied through the normal P1 pins, then this switch should be on.

4. Specifications

Word Size

8- or 16-bits, as determined by the Multibus BHEN signal

Memory Size

131,072 bytes (128K board)

262,144 bytes (256K board)

393,216 bytes (384K board)

524,288 bytes (512K board)

1,048,576 bytes (1M board)

2,097,152 bytes (2M board)

Access/Cycle Time

	CD21/2140		CD21/2141	
	<u>Typical</u>	<u>Maximum</u>	<u>Typical</u>	<u>Maximum</u>
XACK Active	215ns	230ns	155ns	175ns
Data Available	170ns	205ns	135ns	155ns
Cycle Time	--	330ns	--	175ns

Address Selection

DIP switch addressing for each 256K (1 megabyte for boards using 256K RAMs) section to reside on any 256K (1 megabyte) memory boundary in the 16 megabyte address space, plus four row enable jumpers.

Sixteen-bit DIP switch address selection for the I/O port is used, with A8-A15 optionally disconnected.

I/O Port Definition

The data read when accessing the board's I/O port has the following format:

Data Bit 3: 1=Error Occurred
0=No Error

Data Bits 0-2:

<u>Binary Code</u>	<u>Failed Dynamic RAM Section</u>
7	IC1-IC9
6	IC10-IC18
5	IC19-IC27
4	IC28-IC36
3	IC37-IC45
2	IC46-IC54
1	IC55-IC63
0	IC64-IC72

When the I/O port is written, any parity error is cleared.

Interface

All signals meet the IEEE Multibus specification.

IEEE 796 bus compliance: Slave D16 M24 I16

Physical Characteristics

Width: 12.00 in (30.48cm)

Height: 6.75 in (17.15cm)

Depth: 0.5 in (1.27cm)

Weight (512K): 19 oz (539gm)

Electrical Characteristics

Vcc=+5V $\pm 5\%$

Icc=1.8A typical, 2.5A maximum

Environmental Characteristics

Operating Temperature: 0°C to +55°C

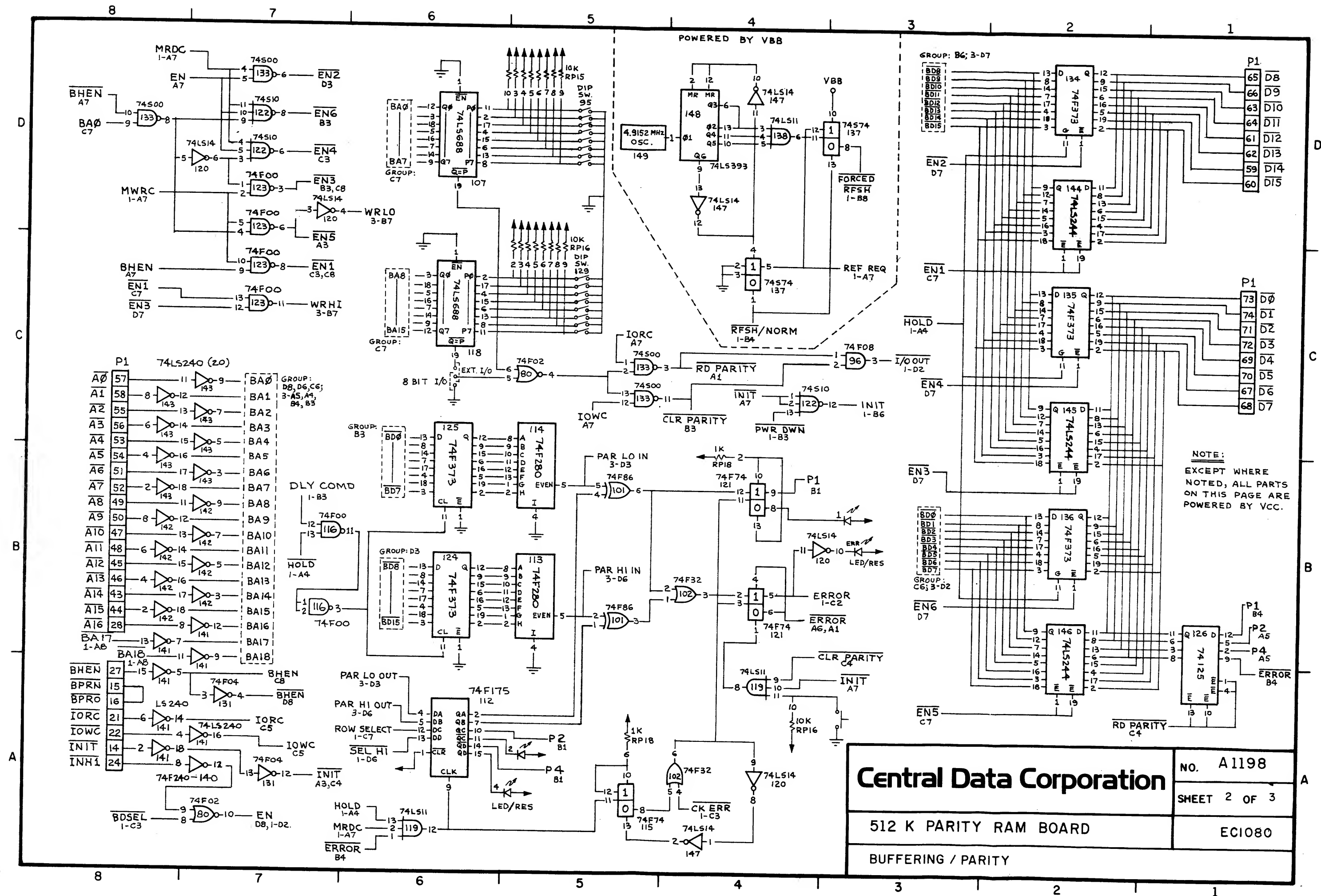
Relative Humidity: 0% to 90% (non-condensing)

Ordering Information

CD21/2140-0128	128K Parity DRAM Board
CD21/2140-0256	256K Parity DRAM Board
CD21/2140-0384	384K Parity DRAM Board
CD21/2140-0512	512K Parity DRAM Board
CD21/2140-Z512	512K Parity DRAM Board, using 256K DRAMs
CD21/2140-1024	1 Megabyte Parity DRAM Board
CD21/2140-2048	2 Megabyte Parity DRAM Board
CD91/2140-HMAN	Hardware Reference Manual
CD21/2141-0256	256K Faster Parity DRAM Board
CD21/2141-0512	512K Faster Parity DRAM Board
CD21/2141-Z512	512K Faster Parity DRAM Board, using 256K DRAMs
CD21/2141-1024	1 Megabyte Faster Parity DRAM Board
CD21/2141-2048	2 Megabyte Faster Parity DRAM Board
CD91/2141-HMAN	Hardware Reference Manual

5. Schematics

The following pages contain the schematics for the 128K-2M Parity Checking Dynamic RAM board. A brief description of the circuitry is given in the Functional Description chapter of this manual.





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